Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An integrated circuit, comprising:

a plurality of inputs;

a plurality of outputs; ~~and~~

a functional block being coupled between the plurality of inputs and the plurality of outputs only in a functional mode of the integrated circuit;

a test arrangement being coupled between the plurality of inputs and the plurality of outputs in a test mode of the integrated circuit, the test arrangement comprising a plurality of logic gates, each logic gate from the plurality of logic gates having a first input coupled to an input from the plurality of inputs; and

a programmable switch configured to switch between the functional mode and the test mode of the integrated circuit, wherein the programmable switch is coupled between an input from the plurality of inputs, the functional block and the first input of each logic gate from the plurality of logic gates,

characterized by each logic gate from the plurality of gates having a further input coupled to a fixed logic value source.

2. (canceled)

3. (original) An integrated circuit as claimed in claim 1, characterized in that the plurality of logic gates comprises exclusive logic gates.

4. (previously presented) An integrated circuit as claimed in claim 1, characterized in that the fixed logic value source is programmable.

5. (previously presented) An integrated circuit as claimed in claim 1, characterized by further comprising a plurality of multiplexers, a multiplexer from the plurality of multiplexers being responsive to a select signal, the multiplexer having a first input coupled to an input from the plurality of inputs, a second input coupled to the fixed logic value source of a logic gate from the plurality of logic gates and an output coupled to the further input of the logic gate.

6. (original) An integrated circuit as claimed in claim 5, characterized in that the select signal is provided by the test arrangement.

7. (original) An integrated circuit as claimed in claim 5, characterized in that the select signal is provided via a dedicated input from the plurality of inputs.

8. (new) An integrated circuit, comprising:

a plurality of inputs;

a plurality of outputs;

a test arrangement being coupled between the plurality of inputs and the plurality of outputs in a test mode of the integrated circuit, the test arrangement comprising a plurality of logic gates, each logic gate from the plurality of logic gates having a first function and a second function, each logic gate from the plurality of logic gates having a first input coupled to an input from the plurality of inputs; and

a plurality of multiplexers, a multiplexer from the plurality of multiplexers being responsive to a select signal, the multiplexer having a first input coupled to an input from the plurality of inputs, a second input coupled to the fixed logic value source of a logic gate from the plurality of logic gates and an output coupled to the further input of the logic gate, wherein the logic gate performs the first function when the multiplexer is switched to the input from the plurality of inputs and the second function when the multiplexer is switched to the fixed logic value source of the logic gate,

characterized by each logic gate from the plurality of gates having a further input coupled to a fixed logic value source.

9. (new) An integrated circuit as claimed in claim 8, characterized by further comprising a functional block being coupled between the plurality of inputs and the plurality of outputs in a functional mode of the integrated circuit.

10. (new) An integrated circuit as claimed in claim 8, characterized in that the plurality of logic gates comprises exclusive logic gates.

11. (new) An integrated circuit as claimed in claim 8, characterized in that the fixed logic value source is programmable.

12. (new) An integrated circuit as claimed in claim 8, characterized in that the select signal is provided by the test arrangement.

13. (new) An integrated circuit as claimed in claim 8, characterized in that the select signal is provided via a dedicated input from the plurality of inputs.

14. (new) An integrated circuit, comprising:

a plurality of inputs;

a plurality of outputs; and

a test arrangement being coupled between the plurality of inputs and the plurality of outputs in a test mode of the integrated circuit, the test arrangement comprising a plurality of logic gates, each logic gate from the plurality of logic gates having a first input coupled to an input from the plurality of inputs;

characterized by each logic gate from the plurality of gates having a further input coupled to a fixed logic value source, wherein the fixed logic value source includes a plurality of subsources, each subsource being arranged to provide the further input of at least one logic gate from the plurality of logic gates with a fixed logic value.

15. (new) An integrated circuit as claimed in claim 14, characterized by further comprising a functional block being coupled between the plurality of inputs and the plurality of outputs in a functional mode of the integrated circuit.

16. (new) An integrated circuit as claimed in claim 14, characterized in that the plurality of logic gates comprises exclusive logic gates.

17. (new) An integrated circuit as claimed in claim 14, characterized in that the fixed logic value source is programmable.

18. (new) An integrated circuit as claimed in claim 14, characterized by further comprising a plurality of multiplexers, a multiplexer from the plurality of multiplexers being responsive to a select signal, the multiplexer having a first input coupled to an input from the plurality of inputs, a second input coupled to the fixed logic value source of a logic gate from the plurality of logic gates and an output coupled to the further input of the logic gate.

19. (new) An integrated circuit as claimed in claim 18, characterized in that the select signal is provided by the test arrangement.

20. (new) An integrated circuit as claimed in claim 19, characterized in that the select signal is provided via a dedicated input from the plurality of inputs.